Si9145

Low-Voltage Switchmode Controller

Features

- 2.7-V to 7-V Input Operating Range
- Voltage-Mode PWM Control
- High-Speed, Source-Sink Output Drive (200 mA)
- Internal Oscillator (up to 2 MHz)
- Standby Mode
- 0−100% Controllable Maximum Duty-Cycle

Description

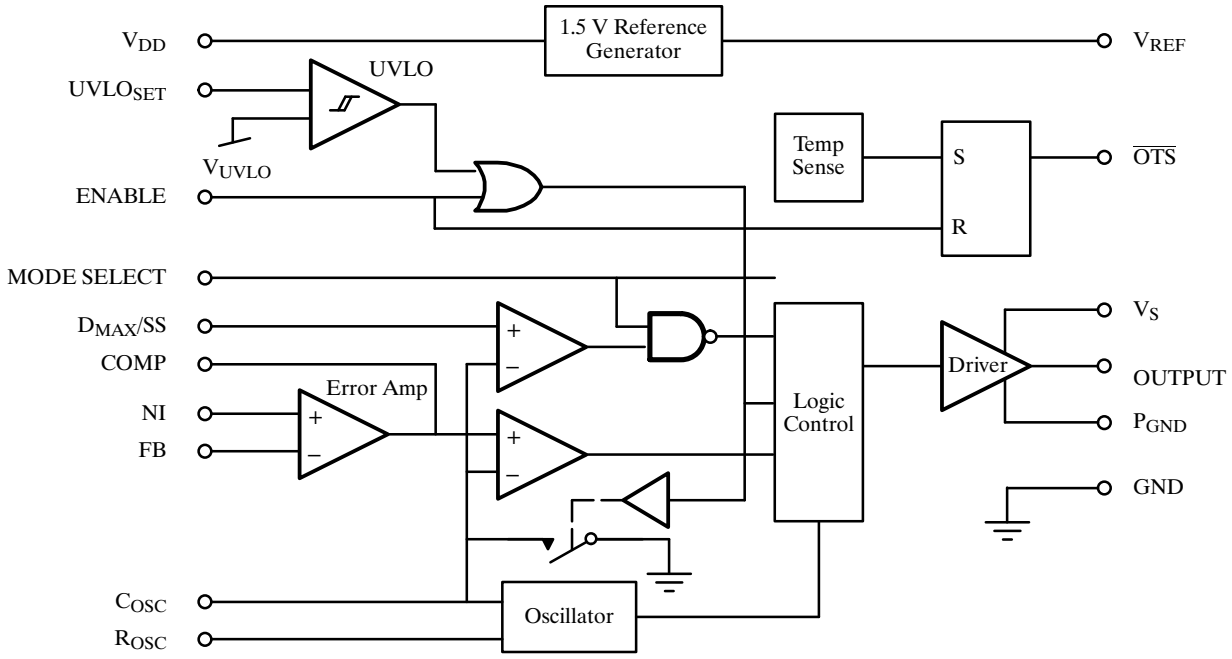
The Si9145 switchmode controller IC is ideally suited for high efficiency dc/dc converters in low input voltage systems. Operation is guaranteed down to 2.7 V, with a minimum start-up voltage of 3.0 V making the Si9145 ideal for use with NiCd, NMH, and lithium ion battery packs. A mode select pin allows the output driver polarity to be programmed allowing the device to function as a step-up or step-down converter.

Features include a precision bandgap reference, a wide bandwidth error amplifier, a 2-MHz oscillator, an input voltage monitor with standby mode and a 200-mA output driver. Supply current in normal operation is typically 1.1 mA and 250 µA in standby mode.

The Si9145 implements conventional voltage mode control. The maximum duty cycle in boost mode can be limited by voltage on D_{MAX}/SS pin. Frequency can be externally programmed by selection of R_{OSC} and C_{OSC}.

The Si9145 is available in 16-pin SOIC and TSSOP packages and is specified over the industrial temperature range (−25°C to 85°C).

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to GND.

V_{DD}, V_S . . . . . 8 V
P_{GND} . . . . . ±0.3 V
V_{DD} to V_S . . . . . −0.3 V
Linear Inputs . . . . . −0.3 V to V_{DD} to +0.3 V
Logic Inputs . . . . . −0.3 V to V_{DD} to +0.3 V
Continuous Output Current . . . . . 100 mA
Storage Temperature . . . . . −65 to 125°C
Operating Junction Temperature . . . . . 150°C

Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] . . . . . 900 mW
16-Pin TSSOP (Q Suffix)[c] . . . . . 925 mW

Thermal Impedance (Θ_{JA})
16-Pin SOIC . . . . . 140°C/W
16-Pin TSSOP . . . . . 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.
c. Derate 7.4 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to GND.

V_{DD} . . . . . 2.7 V to 7 V
V_S . . . . . 2.7 V to 7 V
f_{OSC} . . . . . 2 kHz to 2 MHz
R_{OSC} . . . . . 5 kΩ to 250 kΩ
C_{OSC} . . . . . 47 pF to 200 pF
Linear Inputs . . . . . 0 to V_{DD}
Digital Inputs . . . . . 0 to V_{DD}
V_{REF} Load Resistance . . . . . >150 kΩ

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S GND = P_{GND}		Limits B Suffix − 25 to 85°C Min[b]	Typ	Max[b]	Unit
Reference							
Output Voltage	V_{REF}	I_{REF} = −10 µA		1.455		1.545	V
			T_A = 25°C	1.477	1.50	1.523	
Oscillator							
Maximum Frequency[c]	f_{MAX}	V_{CC} = 3.0 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ		2.0			MHz
Accuracy	f_{OSC}	V_{CC} = 3.0 V C_{OSC} = 100 pF, R_{OSC} = 6.98 kΩ	T_A = 25°C	0.85	1.0	1.15	
R_{OSC} Voltage	V_{ROSC}				1.0		V
Minimum Start-Up Voltage	V_{DDOSC}			3.0			
50% D_{MAX}/SS	V_{DMAX} 50%	MODE SELECT = V_{DD}			1.25		
100% D_{MAX}/SS	V_{DMAX} 100%				1.54		
D_{MAX}/SS Input Current	I_{DMAX}	D_{MAX} = 0 to V_{DD}		−100		100	nA
Voltage Stability[c]	Δf/f	2.7 V ≤ V_{DD} ≤ 7 V, Ref to 4.8 V	T_A = 25°C	−16		16	%
		2.7 V ≤ V_{DD} ≤ 4.2 V, Ref to 3.5 V		−8		8	
		3.8 V ≤ V_{DD} ≤ 5.6 V, Ref to 4.7 V		−7		7	
Temperature Stability[c]		Referenced to 25°C			±5		

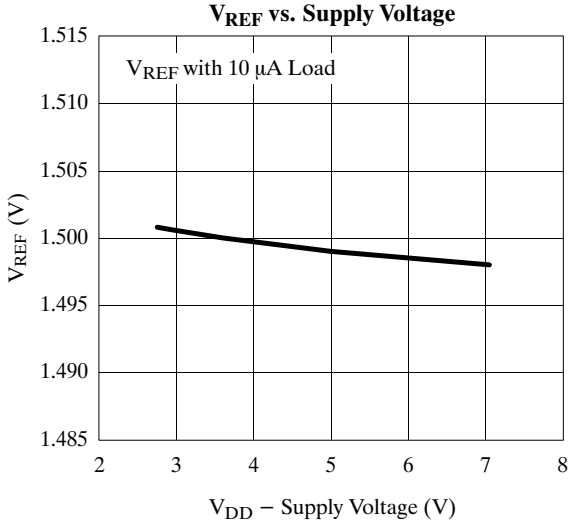
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S GND = P_{GND}	Limits B Suffix − 25 to 85°C Min[b]	Typ	Max[b]	Unit
Error Amplifier (C_{OSC} = GND, OSC DISABLED)						
Input Bias Current	I_{FB}	V_{NI} = V_{REF}, V_{FB} = 1.0 V	−1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	−15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{EA}	Source (V_{FB} = 1 V, NI = V_{REF})		−2.0	−1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	P_{SRR}	2.7 V < V_{DD} < 7.0 V		60		dB
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysterisis	V_{HYS}	V_{UVLOLH} – V_{UVLOHL}		200		mV
UVLO Input Current	I_{UVLO}	V_{UVLO} = 0 to V_{DD}	−100		100	nA
OUTPUT						
Output High Voltage	V_{OH}	V_{DD} = 2.7 V, I_{OUT} = −10 mA	2.55	2.60		V
Output Low Voltage	V_{OL}	V_{DD} = 2.7 V, I_{OUT} = 10 mA		0.06	0.15	
Peak Output Current	I_{SOURCE}	V_{DD} = 2.7 V, V_{OUT} = 0 V		−180	−130	mA
Peak Output Current	I_{SINK}	V_{DD} = 2.7 V, V_{OUT} = 2.7 V	150	200		
Logic						
ENABLE Delay to Output	td_{EN}	ENABLE Rising to OUTPUT		35		ns
ENABLE Logic Low	V_{ENL}				0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}		0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}	−1.0		1.0	µA
MODE SELECT Logic Low	V_{MODEL}				0.2 V_{DD}	V
MODE SELECT Logic High	V_{MODEH}		0.8 V_{DD}			
MODE SELECT Input Current	I_{MODE}	MODE SELECT = 0 to V_{DD}	−1.0		1.0	µA
Over Temperature Sense						
Trip Point	T_{TRIP}			150		°C
Output Low Voltage	V_{OTSL}	V_{DD} = 2.7 V, I_{OUT} = 1 µA		0.06	0.15	V
Output High Voltage	V_{OTSH}	V_{DD} = 2.7 V, I_{OUT} = −1 µA	2.55	2.6		
Supply						
Supply Current − Normal Mode	I_{DD}	V_{DD} = 2.7 V, f_{OSC} = 1 MHz, R_{OSC} = 6.98 kΩ		1.1	1.5	mA
		V_{DD} = 7 V, f_{OSC} = 1 MHz, R_{OSC} = 6.98 kΩ		1.6	2.3	
Supply Current − Standby Mode		ENABLE = Low		250	330	µA

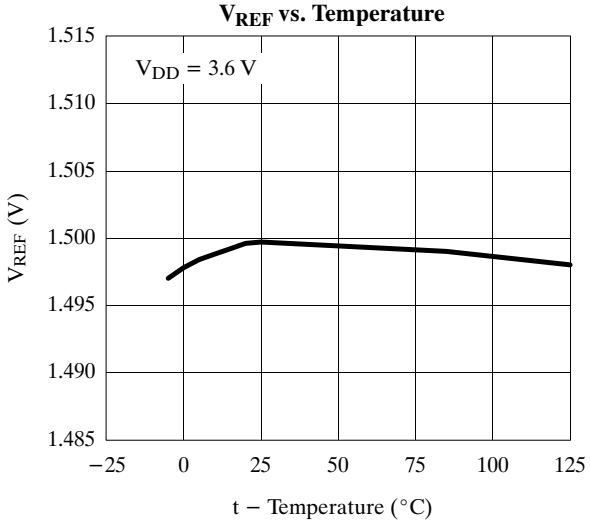
Notes
a. C_{STRAY} < 5 pF on C_{OSC}. After Start-Up, V_{DD} of ≥ 3 V.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

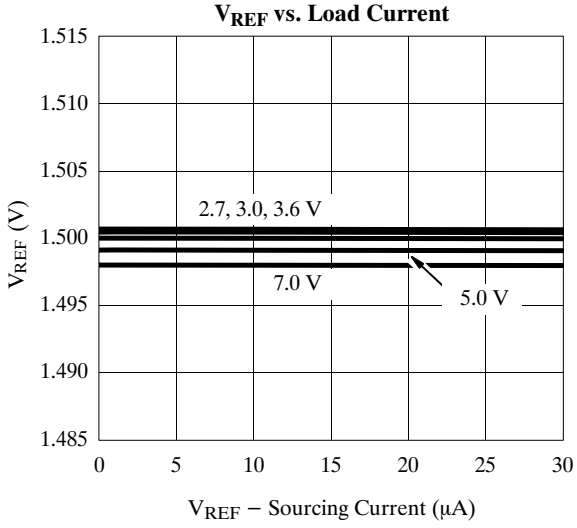
V_{REF} vs. Supply Voltage



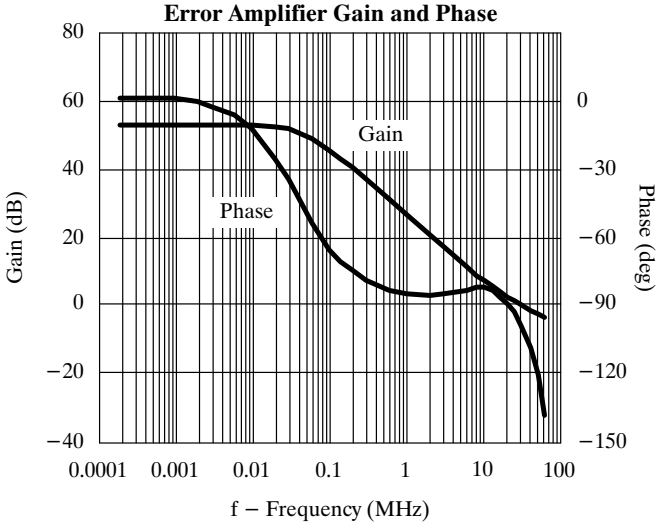
V_{REF} vs. Temperature



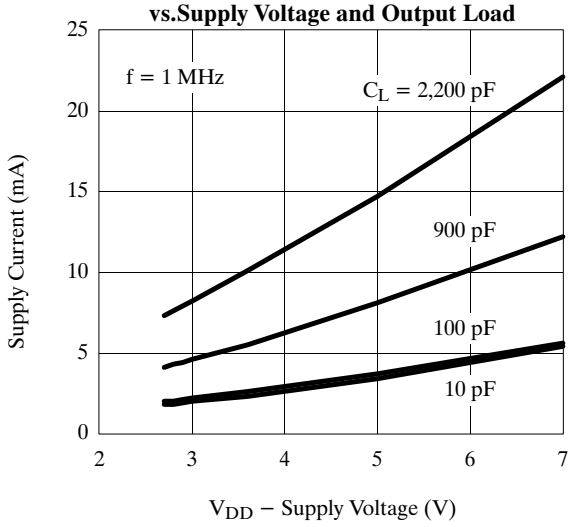
V_{REF} vs. Load Current



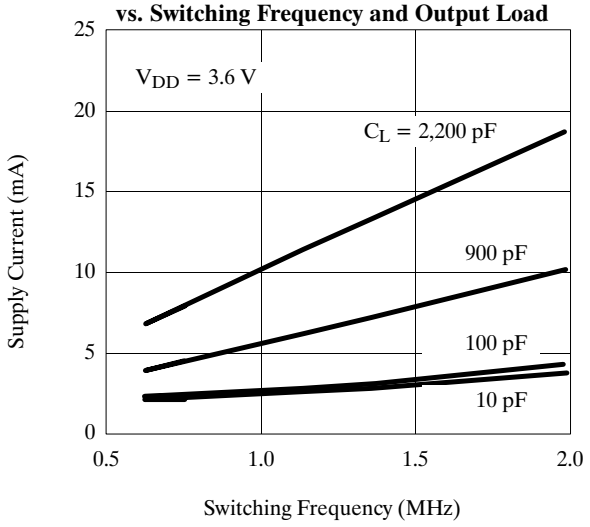
Error Amplifier Gain and Phase



Supply Current vs.Supply Voltage and Output Load

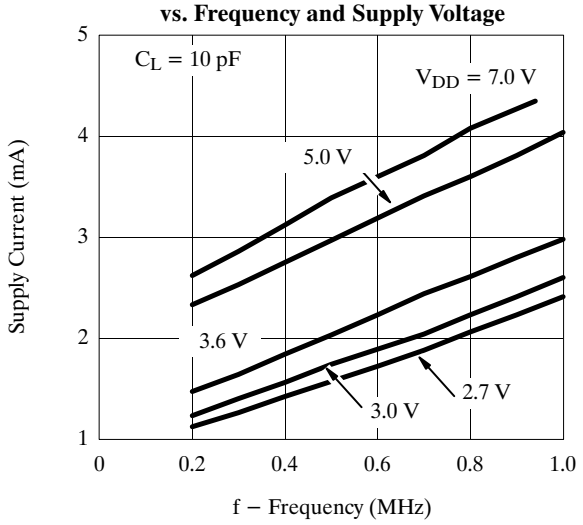


Supply Current vs. Switching Frequency and Output Load

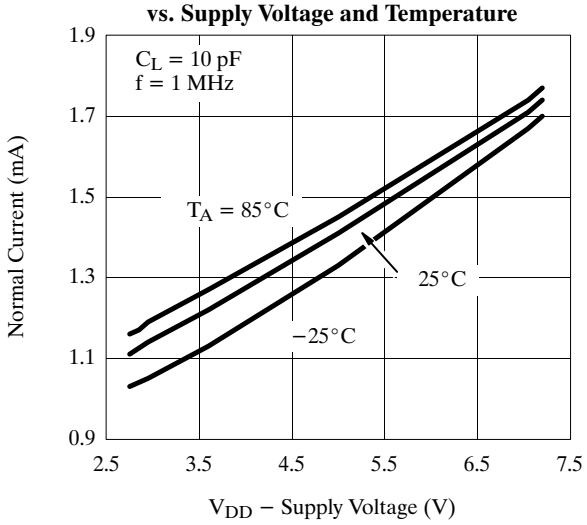


Typical Characteristics (25°C Unless Otherwise Noted)

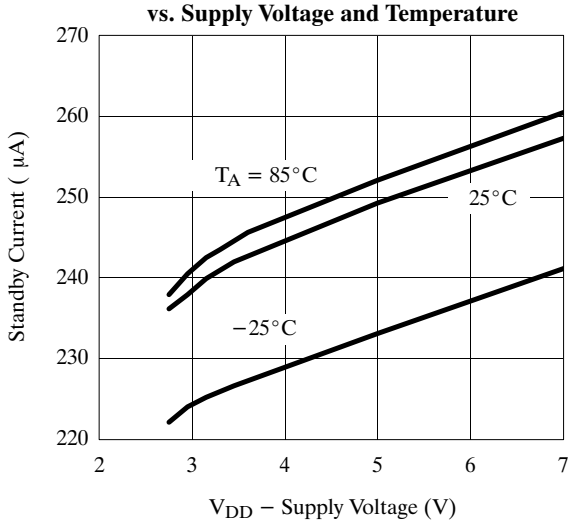
Supply Current vs. Frequency and Supply Voltage



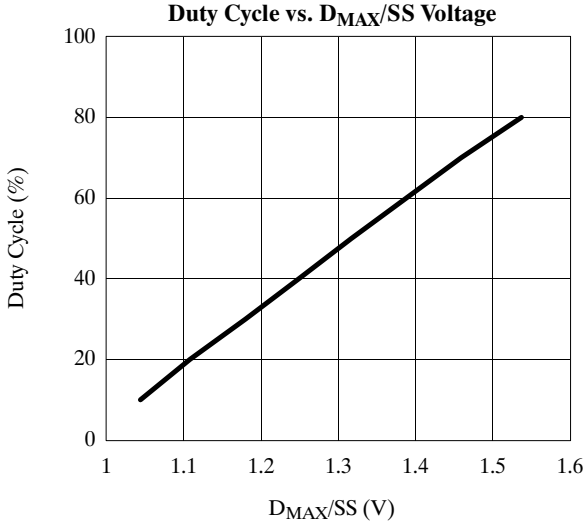
Supply Current vs. Supply Voltage and Temperature



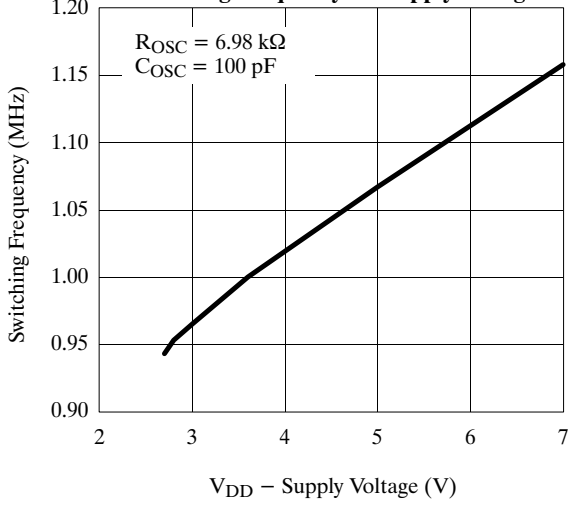
Standby Current vs. Supply Voltage and Temperature



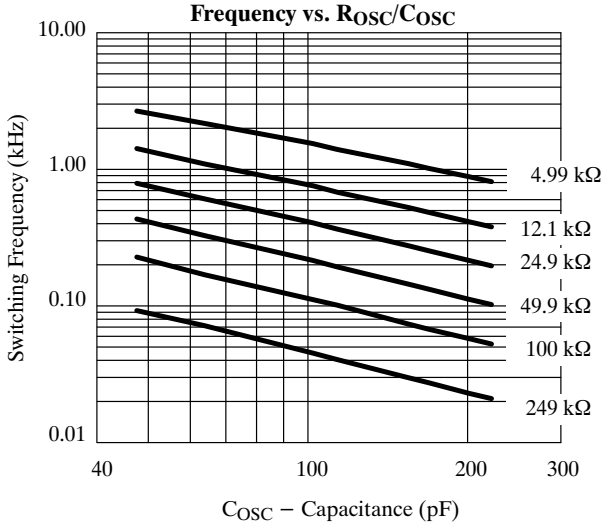
Duty Cycle vs. D_{MAX}/SS Voltage



Switching Frequency vs. Supply Voltage

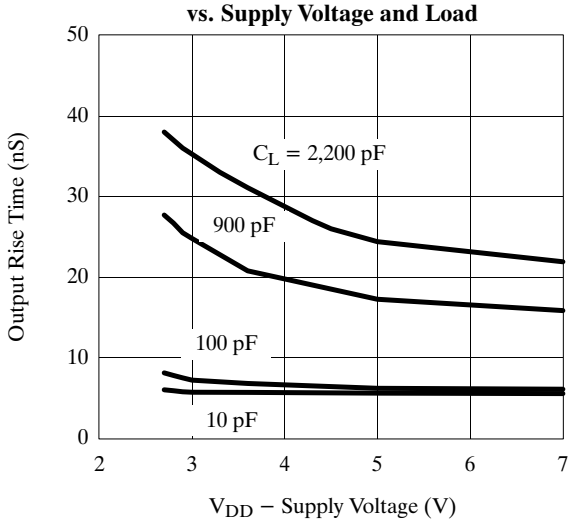


Frequency vs. R_{OSC}/C_{OSC}

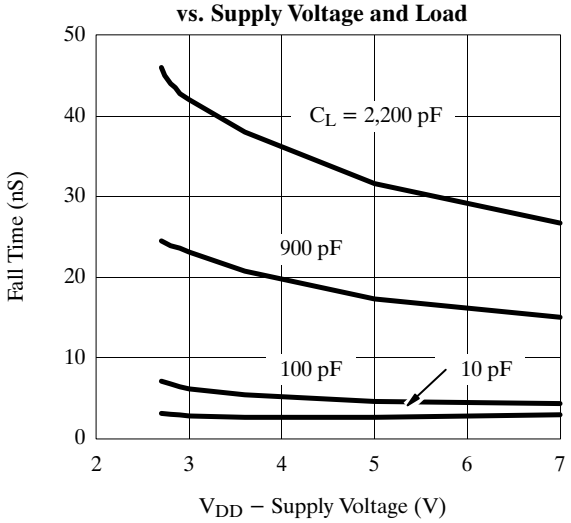


Typical Characteristics (25°C Unless Otherwise Noted)

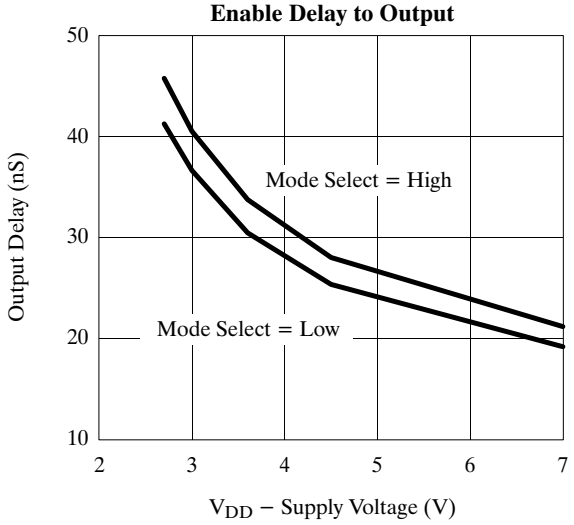
Output Rise Time vs. Supply Voltage and Load



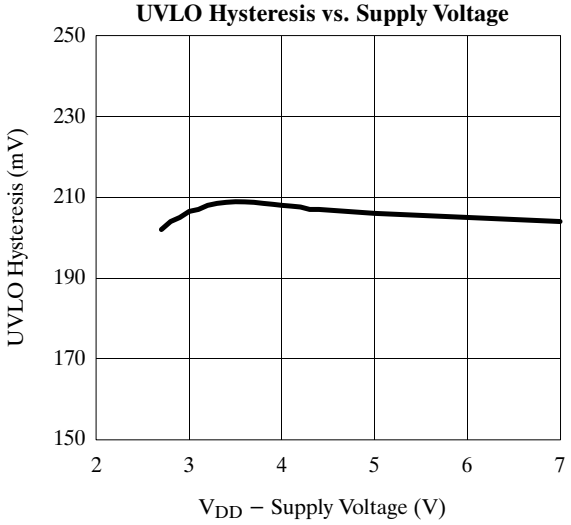
Output Fall Time vs. Supply Voltage and Load



Enable Delay to Output



UVLO Hysteresis vs. Supply Voltage



Timing Waveforms

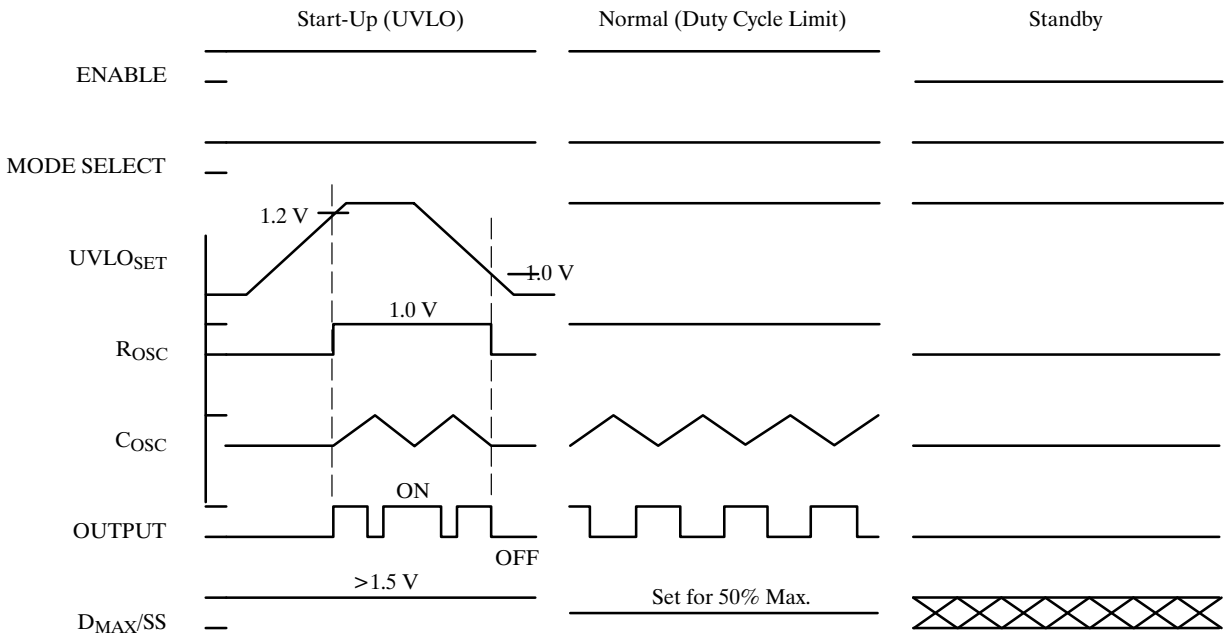


Figure 1. Si9145 Timing Diagram (MODE SELECT = High)

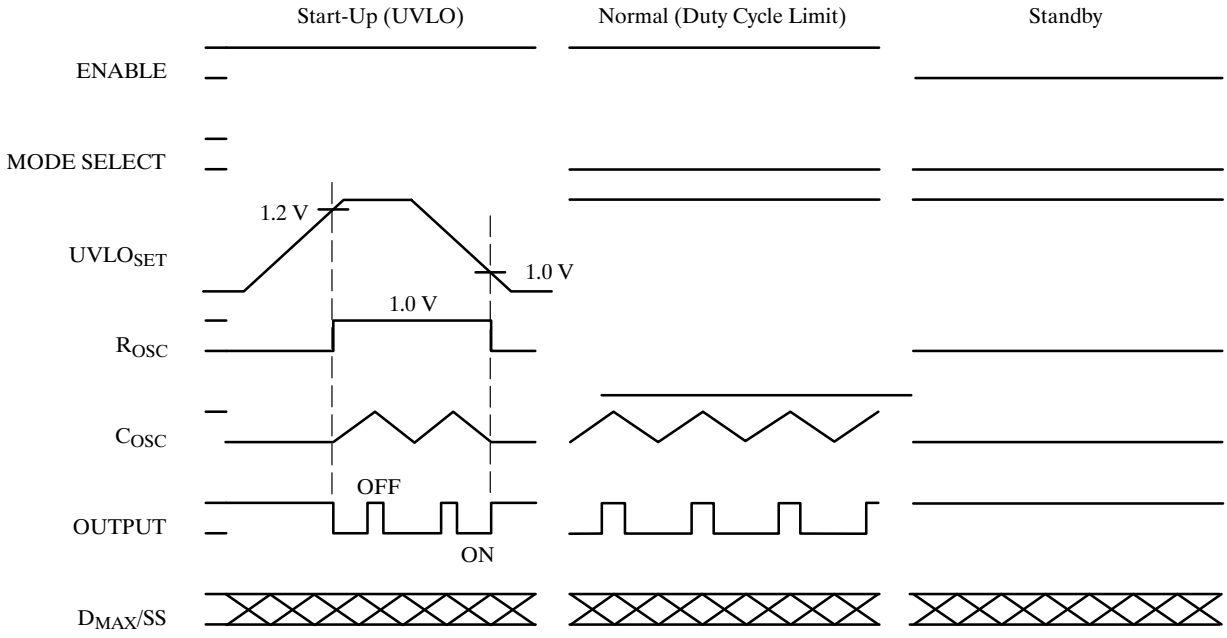
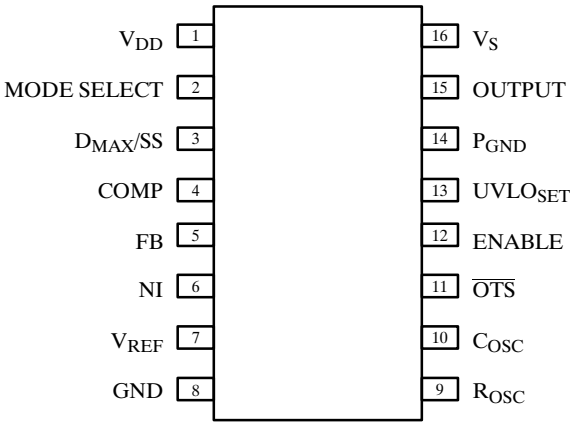


Figure 2. Si9145 Timing Diagram (MODE SELECT = Low)

Pin Configurations

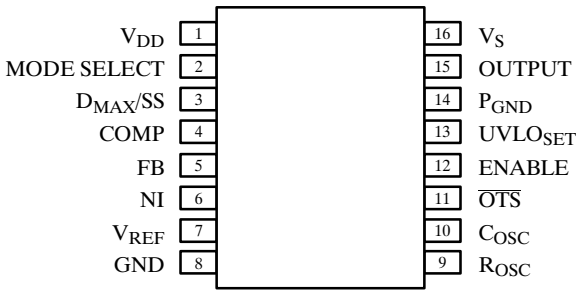
SO-16



Top View

Order Number: Si9145BY

SO-16 (TSSOP)



Top View

Order Number: Si9145BQ

Pin Description

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: MODE SELECT

This pin is used to enable maximum duty cycle limit and set output polarity of controller. When connected to V_{DD}, the maximum duty cycle function is controlled by the D_{MAX}/SS pin. The maximum duty cycle limit is usually used for forward, flyback, and boost converters. The output polarity is high when the PWM circuitry requires the external device to be turned on.

When connected to GND, the maximum duty cycle is not limited (usually for buck converters driving a p-channel MOS). The output polarity is low when the PWM circuitry requires the external PMOS to be turned on.

Pin 3: D_{MAX}/SS

D_{MAX}/SS pin controls the maximum duty cycle achievable by the PWM circuitry when the MODE SELECT = V_{DD}.

When D_{MAX}/SS is at less than 1.0 V (typical) the OUTPUT is held low (0% duty cycle). When D_{MAX}/SS is at more than 1.5 V (typical), the PWM circuitry can achieve 100% duty cycle. With voltage at D_{MAX}/SS between 1.0 V and 1.5 V, the maximum duty cycle is proportionally limited to this voltage.

The addition of external components can implement a soft start function.

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin Description (Cont'd)

Pin 5: FB

The inverting input of the error amplifier. External resistors are connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to the V_{REF} pin.

Pin 7: V_{REF}

This pin supplies 1.5 V trimmed to ±1.5%. The reference voltage is generated by a band-gap reference.

Pin 8: GND

Negative return for V_{DD}.

Pin 9: R_{OSC}

This pin is the equivalent of a 1.0-V voltage source derived from the on-chip V_{REF}. When a low T.C. resistor is externally connected from this pin to GND, a temperature independent current is generated internally. This current is used as the charging current source connected to the C_{OSC} pin. The current is internally multiplied by 2 and is used as the discharging current source connected to the C_{OSC} pin. Therefore, the external resistor is one of the factors that determine the oscillator frequency.

Pin 10: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency. Internal current sources alternately charge and discharge the external capacitor. The oscillator waveform is a symmetrical triangular type with a typical voltage swing between 1.0 V and 1.5 V.

$$f_{osc} \simeq \frac{0.9}{R_{OSC} * C_{OSC}}$$

Pin 11: $\overline{OTS}$

This pin indicates an over-temperature condition on the device when the output is low. The output is latched low and is reset with the ENABLE pin going low then high, or by turning power off and on.

Pin 12: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and the output is held high for MODE SELECT = low, and low for MODE SELECT = high.

Pin 13: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

Pin 14: P_{GND}

The negative return for the V_S supply.

Pin 15: OUTPUT

This CMOS push-pull output pin drives the external MOSFET and is capable of sinking 150 mA or sourcing 130 mA with V_S equal to 2.7 V.

Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output driver. A bypass capacitor is required.

Applications

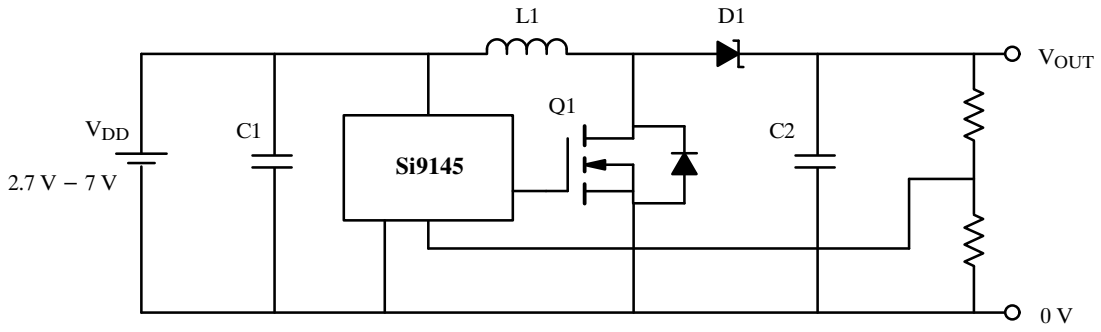


Figure 3. Non-Isolated Step Up Boost Converter for $V_{OUT} > V_{IN}$

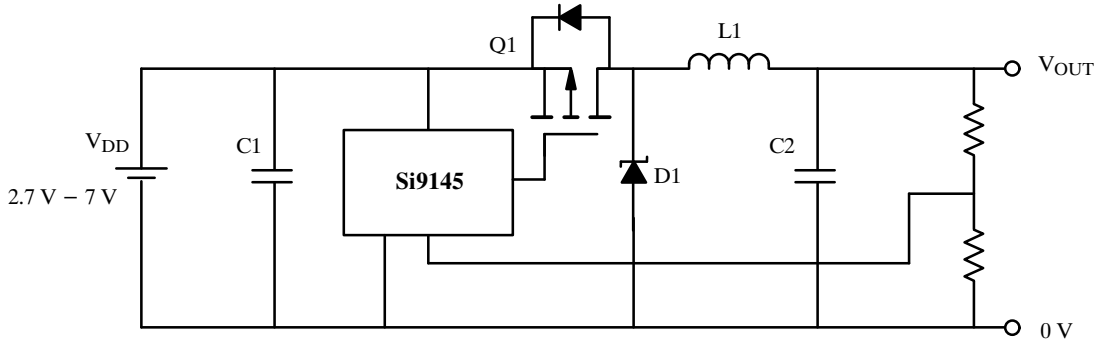


Figure 4. Non-Isolated Step Down Buck Converter for $V_{OUT} < V_{IN}$

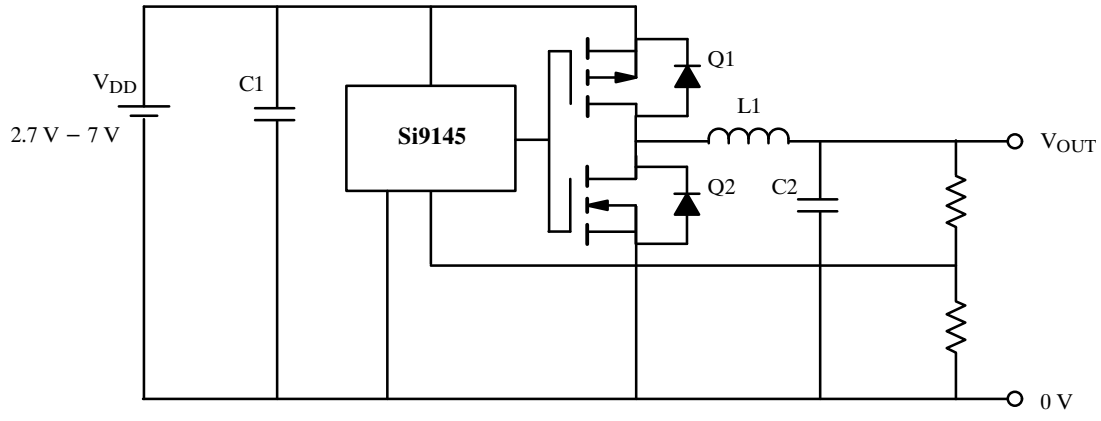


Figure 5. Non-Isolated Synchronous Buck Converter for $V_{OUT} < V_{IN}$